CLAIMS

What is claimed is:

1. A circuit for selectively interconnecting two nodes in an integrated circuit device comprising:

a memory array having a plurality of wordlines and a plurality of bitlines;

a refresh transistor having a source coupled to one of said plurality of bitlines, a control gate coupled to a dynamic random access memory wordline, and a drain;

a switching transistor having a gate coupled to said drain of said refresh transistor, a source coupled to a first one of the nodes and a drain coupled to a second one of the nodes; and

an address decoder for supplying periodic signals to drive said wordlines and said dynamic random access memory wordline.

2. The circuit of claim 1 wherein said memory array drives said bitlines through a sense amplifier and a level-shifting circuit.

3. The circuit of claim 1 wherein said periodic signals have a repetition rate that is a function of temperature of a die on which said circuit is disposed.

4. The circuit of claim 1 wherein said memory array is a flash memory array.

5. A circuit for selectively interconnecting N pairs of nodes in an integrated circuit device comprising:

a memory array having a plurality of wordlines and a plurality of bitlines;

a plurality of dynamic random access memory wordlines;

a separate switch for each pair of nodes in the integrated circuit, each said switch associated with a unique combination of one of said bitlines and one of said dynamic random access memory wordlines, each said switch including a refresh transistor and a switching transistor, said refresh transistor having a source coupled to one of said plurality of bitlines, a control gate coupled to one of said dynamic random access memory wordlines and a drain, said switching transistor having a gate coupled to said drain of said refresh transistor, a source coupled to a first one of the nodes and a drain coupled to a second one of the nodes;

an address decoder having at least N distinct states for supplying signals to said wordlines and said dynamic random access memory wordlines; and

a sequencing circuit for sequencing said address decoder through said at least N states.

6. The circuit of claim 5 wherein said memory array drives said bitlines through a sense amplifier and a level-shifting circuit.

7. The circuit of claim 5 wherein said sequencing circuit sequences said address decoder through said at least N states at a rate that is a function of temperature of a die on which said circuit is disposed.

8. The circuit of claim 5 wherein said memory array is disposed on a first die and the remainder of said circuit is disposed on a second die interconnected to said first die.

9. The circuit of claim 8 wherein said memory array is a flash memory array.

10. The circuit of claim 8 wherein said first die is interconnected to said second die by face-to-face interconnect.

11. The circuit of claim 10 wherein said memory array is a flash memory array.

12. A method for interconnecting two nodes in an integrated circuit device comprising:

storing a charge representing an on-status bit on a gate capacitance of a switching transistor coupled between the two nodes; and

periodically refreshing said charge.

13. The method of claim 12 wherein periodically refreshing said charge comprises periodically coupling a voltage representing said on-status bit to said gate capacitance of said switching transistor through a refresh transistor.

14. The method of claim 13 wherein periodically coupling a voltage comprises periodically coupling a voltage having a magnitude sufficient to turn on said switching transistor without a Vth drop.

15. The method of claim 13 wherein coupling a voltage representing said on-status bit comprises:

retrieving a signal representing said on-status bit from a memory; and

converting said signal into said voltage.

16. The method of claim 13 wherein periodically refreshing said charge is performed at a periodic interval that is a function of temperature of a die on which said circuit is disposed.

17. A method for interconnecting N pairs of nodes in an integrated circuit device comprising:

for each of said N pairs of nodes storing a charge representing an on-status bit on a gate capacitance of a switching transistor coupled between the pair of nodes; and

periodically refreshing each said charge.

18. The method of claim 17 wherein periodically refreshing each said charge comprises periodically coupling a voltage representing said on-status bit to said gate capacitance of each said switching transistor through a separate refresh transistor.

19. The method of claim 18 wherein periodically coupling a voltage comprises periodically coupling a voltage having a magnitude sufficient to turn on each said switching transistor without a Vth drop.

20. The method of claim 18 wherein coupling a voltage representing said on-status bit comprises:

retrieving a signal representing said on-status bit from a memory; and

converting said signal into said voltage.

21. The method of claim 18 wherein periodically refreshing said charge is performed at a periodic interval that is a function of temperature of a die on which said circuit is disposed.